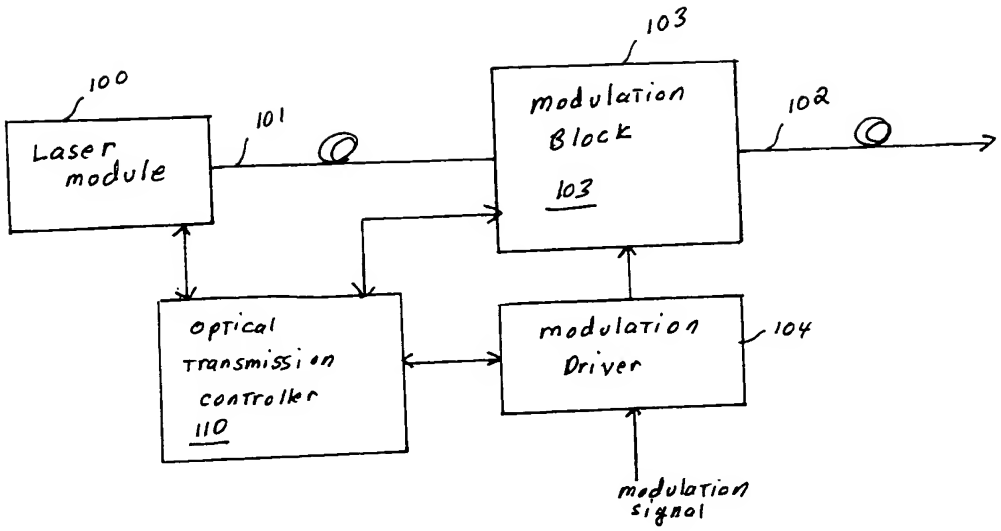

Figure 1

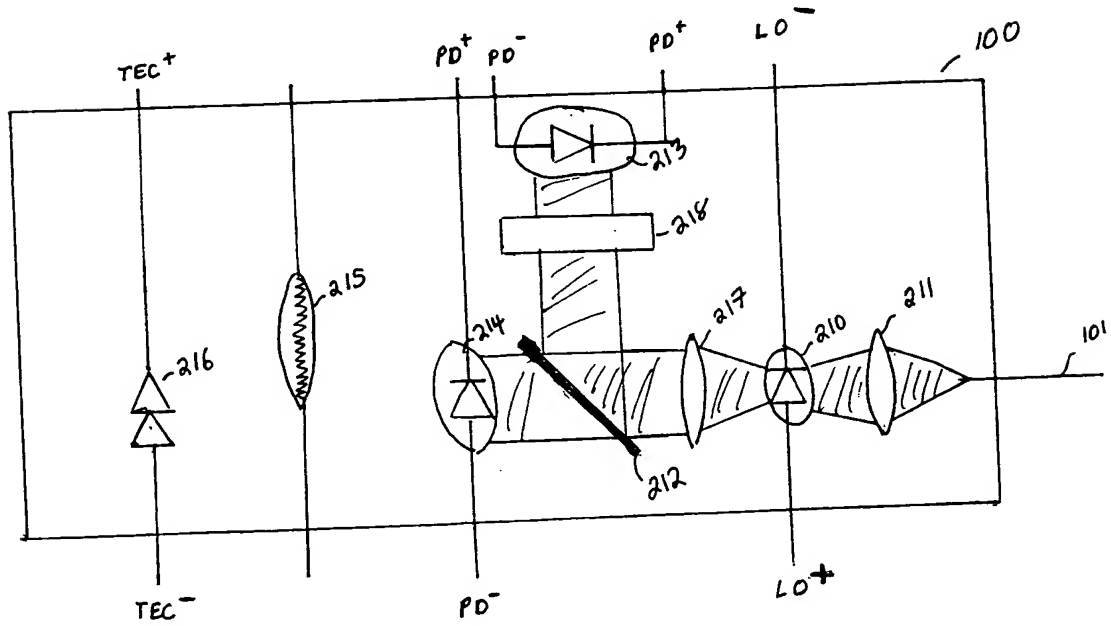

Figure 2

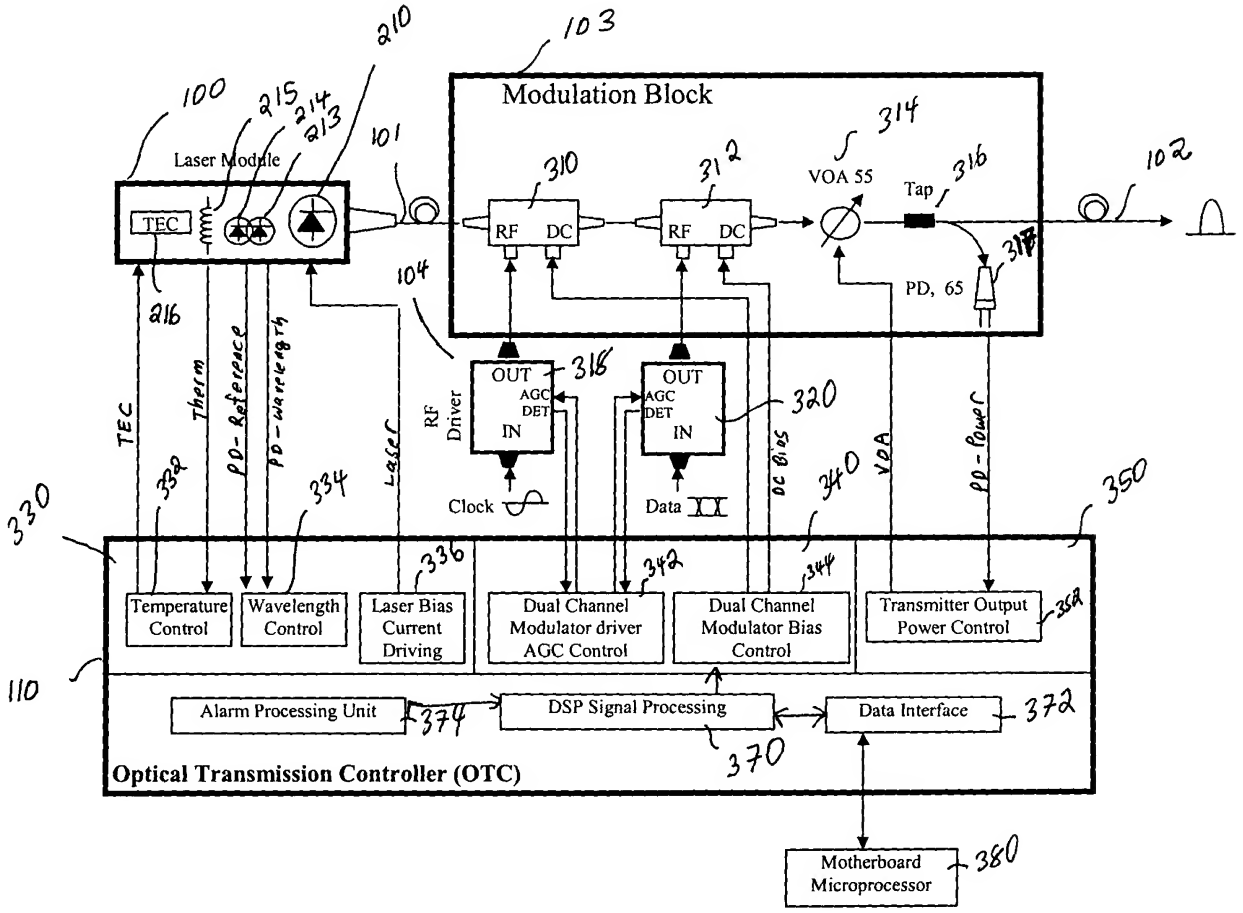
Modulation Block
Laser Module
TEC
RF
DC
VOA 55
Tap
PD, 65
OUT
AGC
DET
IN
RF Driver
Clock
Data
TEC
Therm
PD-Reference
PD-Wavelength
Laser
DC Bias
VOA
PD-Power
Temperature Control
Wavelength Control
Laser Bias Current Driving
Dual Channel Modulator driver AGC Control
Dual Channel Modulator Bias Control
Transmitter Output Power Control
Alarm Processing Unit
DSP Signal Processing
Data Interface
Optical Transmission Controller (OTC)
Motherboard Microprocessor
100
101
102
103
104
110
210
213
214
215
216
310
312
314
316
318
320
330
332
334
336
340
342
344
350
352
370
372
374
380

Figure 3

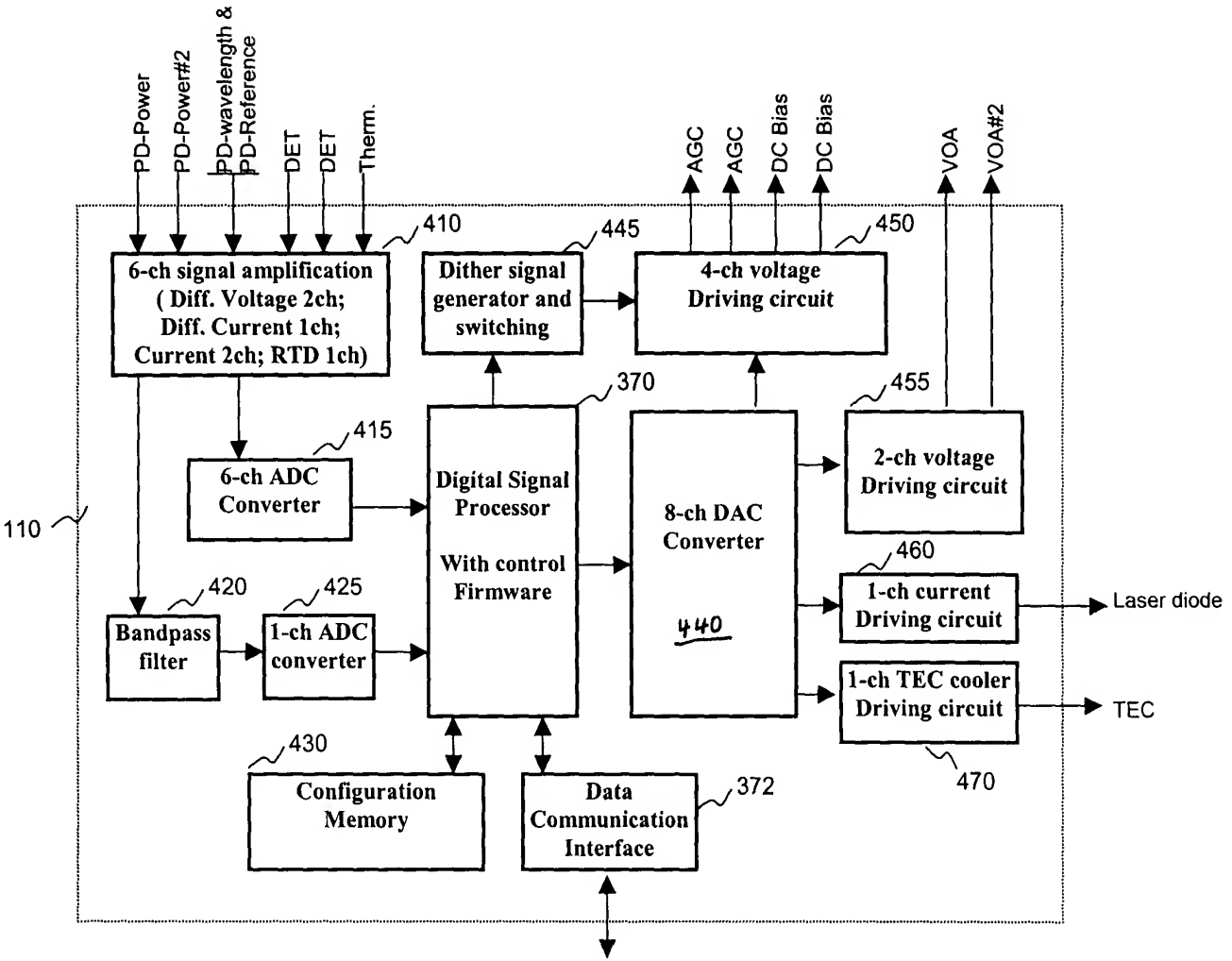
PD-Power
PD-Power#2
PD-wavelength &
PD-Reference
DET
DET
Therm.
AGC
AGC
DC Bias
DC Bias
VOA
VOA#2
410
445
450
6-ch signal amplification
(Diff. Voltage 2ch;
Diff. Current 1ch;
Current 2ch; RTD 1ch)
Dither signal
generator and
switching
4-ch voltage
Driving circuit
370
455
415
6-ch ADC
Converter
Digital Signal
Processor
With control
Firmware
8-ch DAC
Converter
440
2-ch voltage
Driving circuit
110
460
420
425
Bandpass
filter
1-ch ADC
converter
1-ch current
Driving circuit
Laser diode
1-ch TEC cooler
Driving circuit
TEC
470
430
Configuration
Memory
Data
Communication
Interface
372

Figure 4

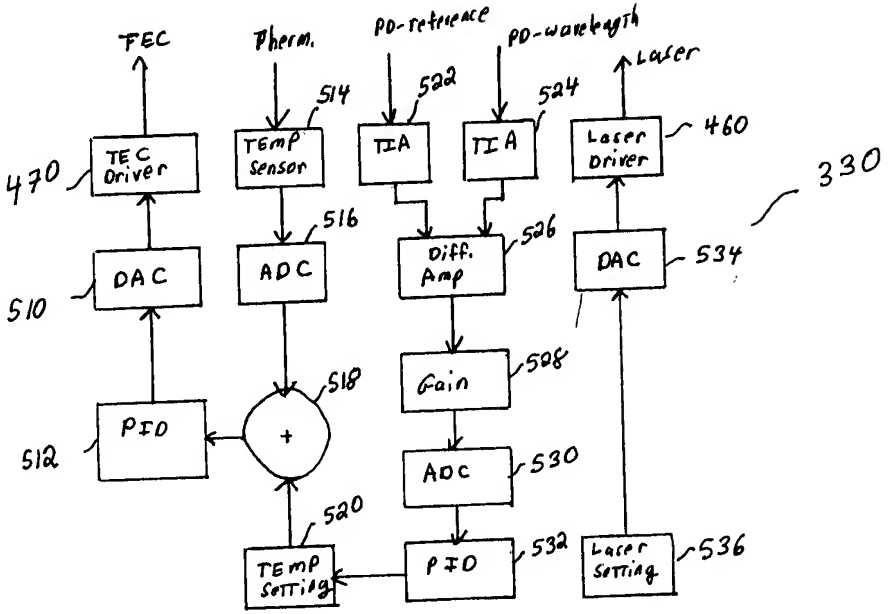
TEC
Therm.
PD-reference
PD-wavelength
Laser
514
522
524
460
470
TEC Driver
Temp Sensor
TIA
TIA
Laser Driver
330
516
526
534
510
DAC
ADC
Diff. Amp
DAC
518
508
512
PID
+
Gain
530
ADC
520
532
536
Temp Setting
PID
Laser Setting

Figure 5A

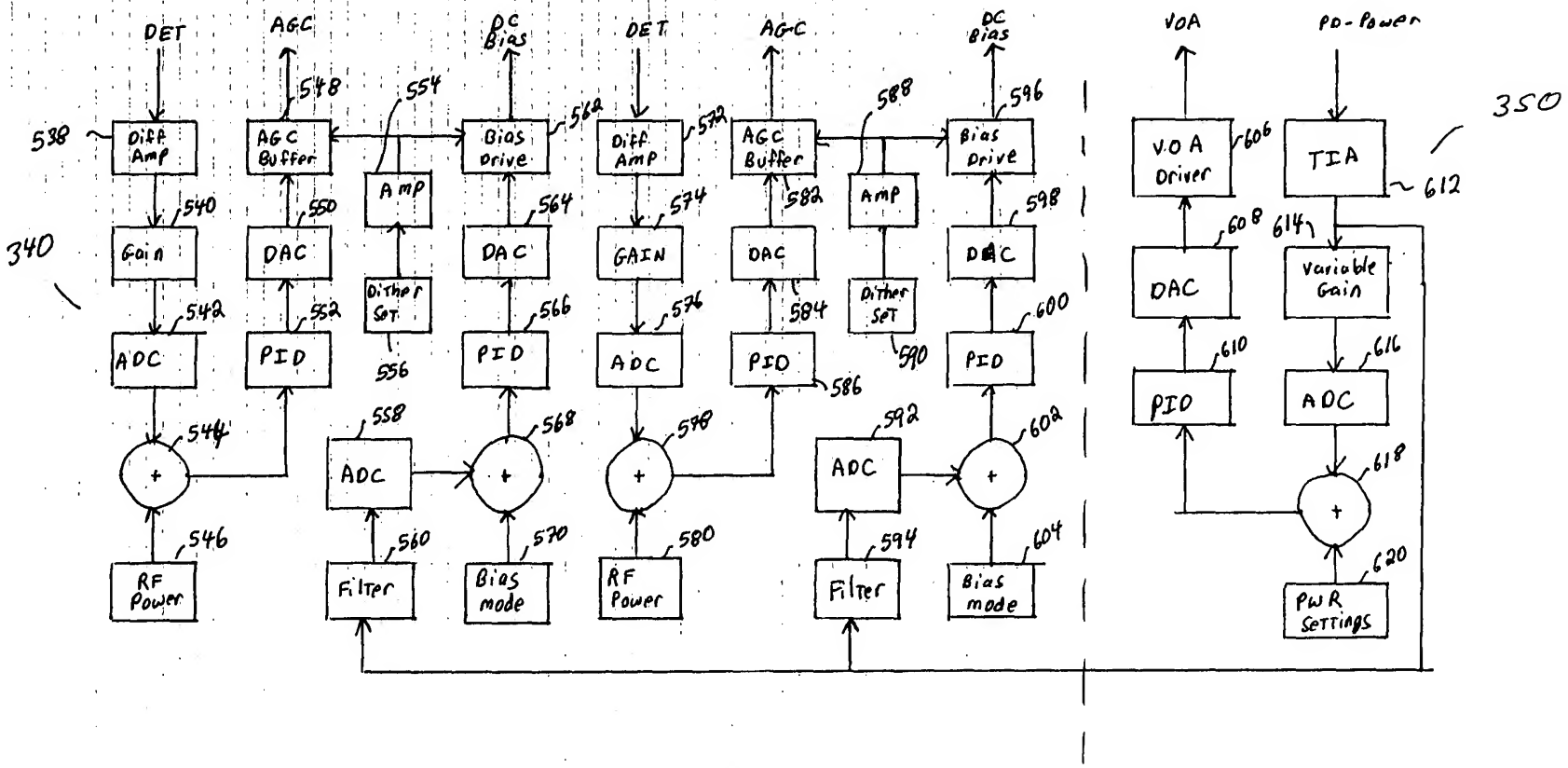
340
350
DET
AGC
DC Bias
538
Diff Amp
AGC Buffer
Bias Drive
540
Gain
DAC
542
ADC
552
PID
544
546
RF Power
548
554
AMP
Dither Set
556
558
ADC
560
Filter
562
564
DAC
566
PID
568
570
Bias mode
572
Diff Amp
574
GAIN
576
ADC
578
580
RF Power
582
AGC Buffer
588
AMP
Dither Set
590
DAC
584
PID
586
592
ADC
594
Filter
596
Bias Drive
598
DAC
600
PID
602
604
Bias mode
VOA
PD-Power
606
V.O.A Driver
608
DAC
610
PID
612
TIA
614
Variable Gain
616
ADC
618
620
PWR Settings

Figure 5B

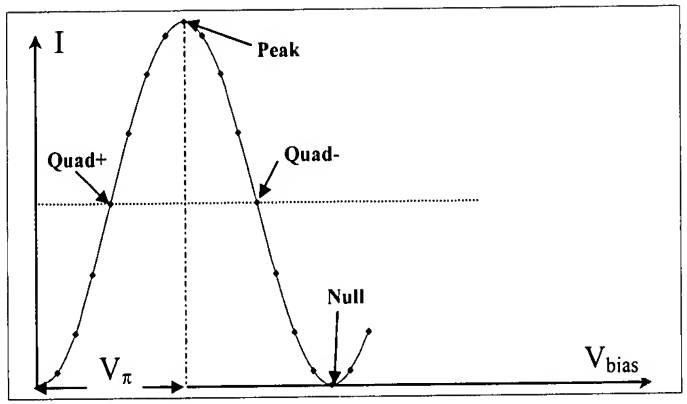

Figure 6

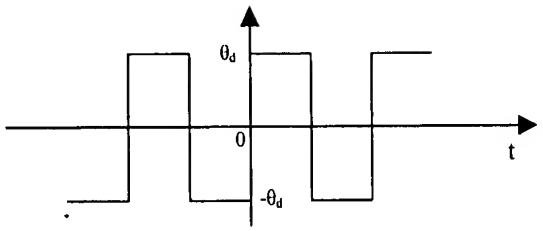

Figure 7A

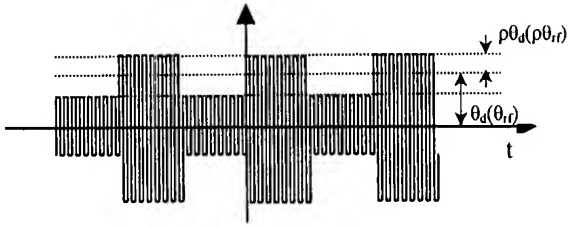

Figure 7B

Bias Mode	RF Driving	Error signal amplitude normalized to P_m
Gated square dither to DC port for Quad+ control	Sinusoidal	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \sin(\rho\,\theta_d) * \text{BesselJ}(0,\theta_{rf})$
	Square Digital	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \sin(\rho\,\theta_d) * \cos\theta_{rf}$
Square dither to modulator driver for Quad+ control	Sinusoidal	$-\rho/\pi * \sin\theta_{dc} * [1-\text{BesselJ}(0, 2\theta_{rf})]$
	Square Digital	$-2/\pi * \sin\theta_{dc} * \sin\theta_{rf} * \sin(\rho\,\theta_{rf})$
Square dither to DC port for Peak control	Sinusoidal	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \text{BesselJ}(0, \theta_{rf})$
	Square Digital	$-2/\pi * \sin\theta_{dc} * \sin\theta_d * \cos\theta_{rf}$

Figure 7C

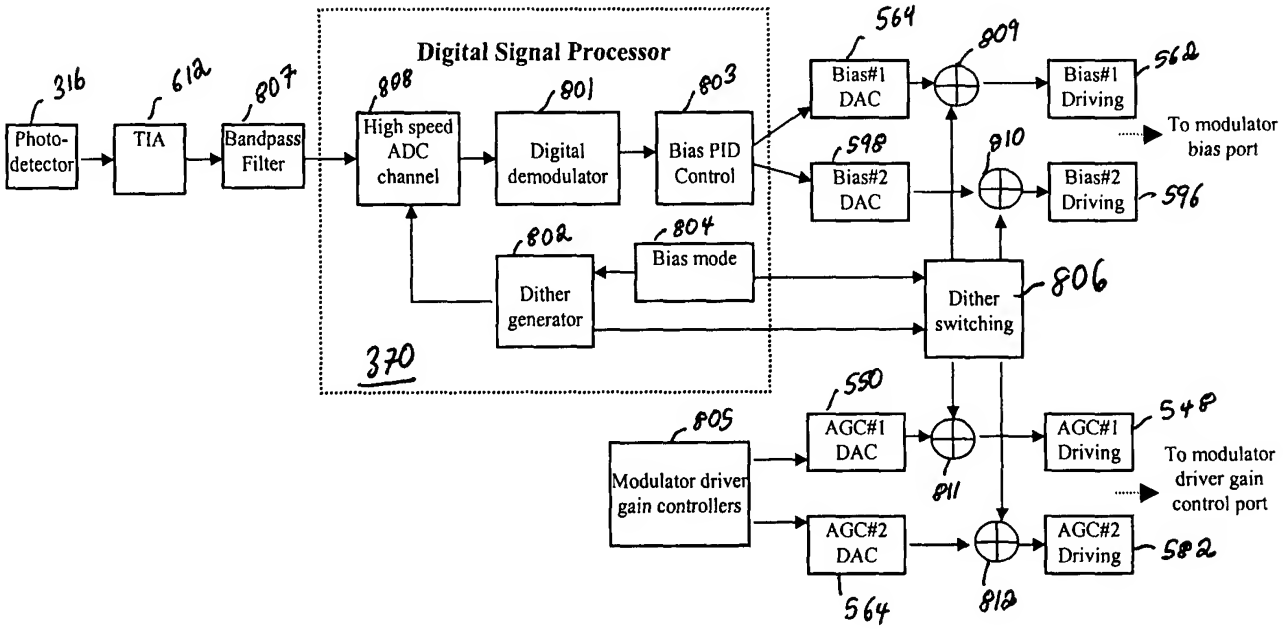
Digital Signal Processor
316
612
807
808
801
803
564
809
562
598
810
596
802
804
806
550
805
548
811
582
812
564
Photo-detector
TIA
Bandpass Filter
High speed ADC channel
Digital demodulator
Bias PID Control
Bias#1 DAC
Bias#1 Driving
To modulator bias port
Bias#2 DAC
Bias#2 Driving
Bias mode
Dither generator
Dither switching
370
AGC#1 DAC
AGC#1 Driving
To modulator driver gain control port
Modulator driver gain controllers
AGC#2 DAC
AGC#2 Driving

Figure 8